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Remarks:
A request for correction of claim 1 has been filed pursuant to Rule 88 EPC. A decision on the request will be taken during the proceedings before the Examining Division (Guidelines for Examination in the EPO, A-V, 3.).

(57) The present invention describes a method of manufacturing a semiconductor device, comprising a semiconductor substrate (2) in the shape of a slice, the method comprising the steps of:
step (1) selectively applying a pattern of a solids-based dopant source to a first major surface of said semiconductor substrate (2);
step (2) diffusing the dopant atoms from said solids-based dopant source into said substrate (2) by a controlled heat treatment step in a gaseous environment surrounding said semi-conducting substrate (2), the dopant from said solids-based dopant source diffusing directly into said substrate (2) to form a first diffusion region (12) in said substrate immediately beneath said pattern of said solids-based dopant source and, at the same time, diffusing said dopant from said solids-based dopant source indirectly via said gaseous environment into said substrate (2) to form a second diffusion region (15) in at least some areas of said substrate (2) not covered by said pattern; and
step (3) forming a metal contact pattern (20) substantially in alignment with said first diffusion region (12) without having etched said second diffusion region (15) substantially.

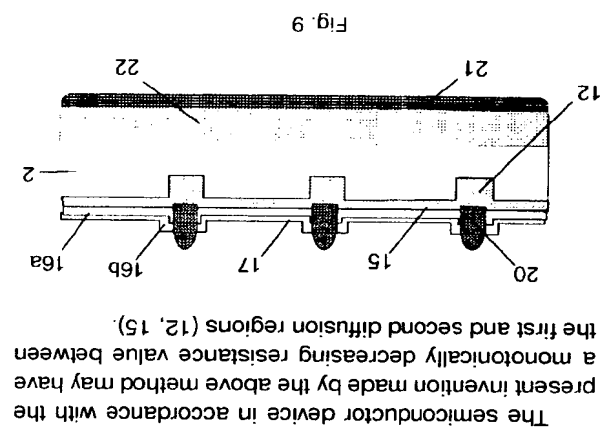


Fig. 9

The semiconductor device in accordance with the present invention made by the above method may have a monotonically decreasing resistance value between the first and second diffusion regions (12, 15).

(54) Semiconductor device with two selectively diffused regions

The method of manufacture according to the present invention is specified in claim 1. The semiconductor device in accordance with the present invention is specified in claim 10.

Summary of the invention

The method of manufacture according to the present invention is specified in claim 1. The semiconductor device in accordance with the present invention is specified in claim 10.

General methods of making photovoltaic devices are described in "Physics, technology and use of photovoltaics" by R. J. Overstraeten and R. P. Mertens, Adam Higler Ltd., 1986 which is incorporated herein by reference.

Known manufacturing methods of a selective emitter/collector using low cost metallisation techniques such as screen printing require a second diffusion step and/or masking and/or etching steps resulting in the need for alignment of the metallisation pattern 3 with the higher doped regions 6 on the front side of the semiconductor device 1.

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Field of the invention

Description

The present invention relates to a semiconductor device and a method for the manufacture thereof, in particular to a photovoltaic cell having two selectively diffused regions produced in a single diffusion step.

Technical background

Many semiconductor devices make use of differently doped regions of the same conductivity type (p or n) to achieve better performance of the device. The formation of these differently doped regions often implies additional process steps that increase the cost of production. A typical semiconductor device 1 is shown in top-view in Fig. 1, which may be a photovoltaic cell, sometimes called a solar cell. A semiconductor substrate 2 of a first doping type has doped surface regions 5, typically of a second doping type, and a metallisation pattern 3 on at least one major surface. The metallisation pattern 3 usually includes elongate metal electrodes 4 between and under which are doped regions 5, e.g. emitter, collector or gate regions. The electrodes 4 may form ohmic contacts to heavily doped regions 6 (shown best in Figs. 3 and 4) of the underlying substrate 2. Electrodes 4 collect from, or supply electric currents to the regions 5, which may include semiconductor devices. For a solar cell, region 5 is usually the emitter region.

Solar cells generally suffer from losses in the emitter region 5. For optimum performance the doping level in the emitter region 5 should be at a low level for optimised photon collection and conversion whereas the regions 6 should be doped strongly and deeply doped to give good ohmic contact to the metallisation pattern 4 without shunting the buried junction 8 (see Figs. 2, 3). Total system cost may be optimised by selecting the best combination of low manufacturing cost with device losses.

A homogeneous emitter/collector design for a solar cell as shown schematically in cross-section in Fig. 2 having front metal contacts 4 back metal contacts 9, a diffusion region 7 and a junction 8. The same diffusion region 7 over the whole front side combined with a low-cost metallisation technique such as screen printing of front metal contacts 4 leads to considerable efficiency losses. This is because the diffusion profile of diffusion region 7 (dopant surface concentration and emitter/collector depth from the surface to the junction 8) required to form good ohmic contacts with this metallisation technique is not ideal for the conversion of light to electrical energy in the intermediate emitter/collector regions 5.

A typical homogeneous emitter/collector process sequence usually incorporates a structuring and chemical preparation of the water surfaces, a diffusion step (in-diffusion of a dopant from the surface/s), an optional

semiconductor substrates with different doping levels. The advantageous design of a selective emitter or collector structure is realised without any additional process step or complication of the process in comparison with homogeneous emitter/collector structures. The most favourable process sequence makes use of screen printing a solids based dopant paste to form the diffusion regions by a first high temperature heat treatment step and screen printing a metal paste to provide the metallisation by a second high temperature heat treatment step.

The selective emitter or collector process in accordance with the present invention, for example for a photovoltaic device, may have the same number of process steps as a typical homogeneous emitter/collector process and less steps than for a conventional selective emitter/collector process. The method of the present invention provides a simple and economical manufacturing method for photovoltaic devices which have advantageous results over known homogeneous emitter/collector structures. Less dopant source material is required as compared with the homogeneous emitter/collector process, thus reducing the production cost while improving the final cell performance.

The present invention is a simplification of known selective emitter or collector formation process sequences. The selective emitter or collector structure in accordance with the present invention is formed within only one diffusion step. No additional masking and/or etching process steps are needed to form the selective emitter or collector.

Brief description of the drawings

Fig. 1 shows a schematic top view of a known semiconductor device.

Fig. 2 shows a schematic cross-section of a known solar cell with a homogeneous emitter/collector structure.

Fig. 3 shows a schematic cross-section of a known solar cell with a selective emitter/collector structure.

Fig. 4 shows a schematic cross-section of a further known solar cell with a selective emitter/collector structure.

Figs. 5 to 10 show schematic steps in the manufacture of a semiconductor device in accordance with an embodiment of the present invention.

Fig. 11 shows schematically the direct and indirect diffusion process in accordance with the present invention.

Fig. 12 shows a plot of the lateral spreading resistance of a semiconductor device in accordance with the present invention.

Figs. 13 to 16 show schematic steps in the manufacture of a semiconductor device in accordance with a further embodiment of the present invention.

Description of the illustrative embodiments

In the following the invention will be described with reference to certain specific embodiments and with reference to the drawings but the invention is not limited thereto but only by the claims. In the drawings some of the dimensions, for instance the thickness of layers, may have been exaggerated for purposes of clarity. In particular, the invention will be explained with reference to a photovoltaic device, sometimes called a solar cell, but the invention is not limited thereto but may find application in semiconductor devices generally. Further, the invention will mainly be described with reference to the formation of differentiated n++ and n+-type regions in a p-type substrate. The invention is not limited thereto. The methods of the present invention may be applied to the formation of differentiated p-type regions in an n-type substrate or the formation of n++ and n+-type regions in an undoped or n-type substrate or p++ and p+-type regions in an undoped or p-type substrate. Further, the invention will mainly be described with reference to a monofacial solar cell but the invention may be applied equally well to a bifacial solar cell.

The use of the simple process in accordance with the present invention to form for instance an emitter or a collector with differently doped regions with only one high temperature step and without using etching or masking techniques is not limited to solar cells. The technique can be used in other micro-electronic production processes as long as there are similar tolerances in the lateral size of doped regions and metal contacts and the diffusion profiles. Photodetectors and microengineered sensors of all types, heat conversion semiconductor devices as well as semiconductor devices of all types such as thyristors are other devices where a reduction of the production cost may be achieved by using the method in accordance with the present invention.

Figs. 5 to 10 show schematically a selective emitter or collector manufacturing process in accordance with the present invention as applied to a solar cell 1. In a low-cost production process in accordance with the present invention, the processing may start with an as-cut semiconductor substrate 2. The substrate 2 may be single crystalline, polycrystalline or amorphous silicon. The quality of the substrate may be less than required for transistor devices, for instance solar grade silicon as disclosed in "Solar cells" 1992, by Martin Green, University of New South Wales. No limits are expected with respect to the size of substrate 2, and the size will depend upon commercially available materials. At the present time 10 cm x 10 cm silicon substrates with a thickness of 200 to 400 micron are used but the invention is not limited thereto. The substrate 2 in accordance with the present invention is preferably silicon but the invention is not limited thereto. The substrate 2 may be GaAs or any other similar semiconductor substrate 2 which requires adjacent diffused doped regions with a

similar variation in the dopant atom concentration in these areas. In a complete device, the deeply diffused regions 12 and the shallow diffused regions 15 would alternate periodically showing a steep gradient at the transition regions where there is roughly one order of magnitude difference in the surface concentration of dopant atoms. The higher the dopant concentration the lower the electrical resistance. The monotonic decrease in dopant concentration and associated electrical resistance from the weakly doped regions 15 towards the deeply diffused regions 12 where the metal contacts 20 will be placed in a finished solar cell provides excellent carrier collection properties. The increasing gradient in the surface concentration of dopant atoms towards the regions where the metal contacts will be placed in the finished solar cell facilitates the carrier transport towards these collecting contacts 20. In accordance with the present invention a monotonic increase of dopant atom density may be obtained in the surface region of the substrate 2 between the shallow regions 15 and the deep regions 12 with at least a fivefold, and typically an order of magnitude or more, difference between the dopant density in the shallow regions 15 and the dopant density in the deep regions 12. It is possible to produce solar cells with the processing sequence of this invention with up to >1% absolute higher efficiencies as compared to solar cells produced by a homogeneous emitter or collector process without adding any process step and while reducing the cost (dopant source) of the diffusion sequence.

After the diffusion step the remaining diffusion glass on the silicon substrate surface may be removed in an chemical etching solution of about 25%-50% HF in DI water and the substrate 2 is cleaned and rinsed afterwards. The present invention includes that the diffusion glass is optionally not removed and the process continues to an oxidation/passivation step. This may avoid an HF acid cleaning step which is an advantage environmentally.

As shown schematically in Fig. 7, the diffusion sequence may be followed by an optional oxidation step where an SiO_2 layer 16a and 16b is formed on the surfaces of the substrate by exposing the substrates to an O_2 atmosphere, typically in a quartz boat, for 1 - 20 minutes at temperatures ranging from 800 - 950 degree C. This SiO_2 layer 16a, 16b serves to passivate defects in the surface emitter/collector region 15 of the substrate 2 which could decrease the solar cell performance. Passivation using an oxide layer reduces the surface recombination velocity which reduces the loss of carriers, hence improving efficiency. Optionally, not only a passivating layer 16a, 16b such as an oxide may be applied but also an anti-reflection coating layer (ARC) 17. The ARC layer 17 may be applied by chemical vapour deposition (CVD, e.g. a TiO_2 layer) or plasma enhanced CVD (PECVD, e.g. a silicon nitride layer) or similar techniques.

Finally the metallisation sequence comprises usu-

ally two or three contact printing steps: front contact 20 and one or two back contact patterns 21 depending on how many different metals are used. As shown schematically in Fig. 8, metal paste 18 is selectively applied to the front side of the substrate 2 in alignment with regions 12 that are heavily doped. A further metal paste 19 is applied either selectively or non-selectively to the backside of the substrate 2. Screen printing and subsequent drying is the most preferred way to apply these contacts, however other thick film techniques mentioned above or evaporation may be used instead. Each printing step is followed by a drying step at moderate temperatures around 250 degree C, e.g. by infra-red heaters. As shown in Fig. 9, the metal pastes 18, 19 are then sintered at high temperatures ranging from 650 to 900 degree C for typically about 30 to 200 seconds to form good ohmic contacts 20 on the front side of the substrate 2 without shunting the junction 8, as well as good ohmic contacts 21 on the back side of substrate 2. The contacts 20 and 21 are formed through any ARC or oxide layer 16b; 17. The peak temperature and temperature profile (temperature versus time) are very important and have to be adapted for each metallisation paste and process sequence separately. Typically the front side and back side contacts screen-printed with metal paste 18, 19 are both sintered together in one high temperature step after having been dried separately. Optionally, a back surface field (BSF) layer 22 is formed at the same time on the back side of substrate 2 as shown schematically in Fig. 9. To form a BSF 22 it is preferred if a high temperature and aluminium paste are used for back surface metal contacts 21.

Optionally, as shown schematically in Fig. 10, an anti-reflection coating (ARC) layer 23 can be applied after metallisation rather than the ARC layer 17 applied before metallisation and described with reference to Fig. 8. Typical ARC layers may include TiO_2 , Si_3N_4 , or Ta_2O_5 , or similar materials and can be applied by various techniques. Metal contact sintering temperatures as high as 800 °C can be used for the contact formation without shunting the junction 8. Where aluminium is used for the metal contacts, sintering at such high temperatures has additional advantages as for instance Al gettering and BSF formation.

Thick film techniques for applying the metal and/or doping pastes such as screen printing show an excellent repeatability. The substrates 2 may be loaded each time by the screen printer into the same position under the screen by means of a CCD camera controlled positioning system. Alignment of metallisation and diffusion patterns can be controlled if oxide and/or ARC layers 16a, 16b; 17, 23 have been applied by utilising the different colour of the slightly wider first diffusion regions 12 under the microscope. With deposition of an ARC layer 17, 23, the substrate 2 shows a different colour at those places where the substrate has higher dopant surface concentrations. This is because the underlying oxide layer 16b grows thicker at places with higher

dopant surface concentration compared with the oxide layer 16a over the areas 15 of lower doping level. As long as the anti-reflective coating (ARC) layer 17 or 23 is applied, the underlying pattern will be visible. The reason for this is a faster oxidation at places with higher dopant surface concentration, resulting in a thicker oxide layer 16. After applying an ARC layer 17 or 23 this difference in oxide thickness becomes visible as a difference in optical thickness and therefore colour of the layers 16b + 17 or 23 compared to 16a + 17 or 23.

It is possible to form with the simple process sequence according to the present invention selective emitter/collector solar cells with improved cell performance (collection efficiency) without complicating the process or increasing the production cost. The result is a more cost-effective production of solar cells. No additional or complicated processing equipment is needed where screen printed diffusion was already used. At the same time the process tolerance is increased by using a selective emitter. Variation in different process parameters as for instance in the metallisation sintering step is less critical than in a homogenous emitter or collector process. This results in a higher process yield which makes the process more cost-effective.

Figs. 13 to 16 show schematically the manufacturing steps of a semiconductor device 30 in accordance with a further embodiment of the present invention. As one embodiment of the present invention has been described in some detail with reference to Figs. 5 to 10, the description of the further embodiment will not be made in detail. The formation of passivation layers, cleaning steps and other details of the process other than the main doping steps will not be described. The process of the further embodiment is suitable for forming a photovoltaic device.

As shown in Fig. 13, a first doped paste pattern 31 is applied selectively to a semiconductor substrate 2 which may be a silicon substrate and may be undoped or may be p-type or n-type conductivity. The paste 31 may be applied by any of the thick-film techniques described previously. The paste pattern 31 is then dried. The first dopant paste 31 may have either the first or second conductivity. The first paste pattern 31 is optionally protected by applying a layer of another material, e.g. a further paste 32. Paste 32 may have a different concentration or type compared with paste 31 or may be undoped. Paste 32 may be applied over a major surface of substrate 2. The paste layer 32 is then dried.

As shown in Fig. 14, a third paste pattern 33 is optionally applied selectively to a further major surface of the substrate 2. Paste pattern 33 is then dried. Paste 33 may have either the first or second conductivity. Paste pattern 33 and other selected parts of the surface of substrate 2 may be protected by the selective application of an undoped material 34, which may be a paste. The paste 34 may be applied by any of the thick-film techniques mentioned above. Paste pattern 34 is then dried.

As shown in Fig. 15, another doped paste pattern 35 may be applied selectively to a major surface of the substrate 2. Paste 35 may include dopant of either conductivity type. Paste 35 may be applied by any of the thick-film techniques mentioned above. Paste pattern 35 is then dried.

The patterned substrate 2 is then placed in a furnace and the dopants from those pastes containing dopant atoms, e.g. 31, 33, 35, are driven into the substrate 2 to form doped layers 37, 39 and 41, respectively. At the same time the dopant atoms from the non-protected pastes diffuse indirectly into regions 42 of the substrate which are not protected to form shallow weakly doped regions 42. Finally, metal pastes are applied in alignment with the regions 37, 39 and optionally 41 and sintered at high temperature to form metal contacts 36, 38, and optionally 40, respectively.

In the process of the further embodiment, substrate 2 may be p-type silicon, pastes 31, 35 and optionally 32 may be phosphorous containing pastes, paste 33 may be a boron paste and paste 34 may be undoped. Paste 32 may be omitted. The device produced with a single diffusion step in accordance with the further embodiment of the present invention may be a solar cell having a selective emitter on the top side and a floating junction on the back side. Such a photovoltaic device may show a better cell performance than a monofacial cell with a conventional back side metallisation over the whole back surface. The device produced by the method of the further embodiment may be used in addition as a bifacial solar cell.

The process in accordance with the further embodiment has the advantage that solar cells can be produced having improved efficiency values and short circuit currents resulting from a more ideal emitter/collector structure and a more ideal back contact. The back contact in accordance with the further embodiment does not have metallisation over the whole of the back major surface of the substrate 2 resulting in better back surface reflection or to its use in bifacial cells designs.

While preferred embodiments of this invention have been described in detail above, it is to be understood that many changes and modifications may be made by those skilled in the art without departing from the scope and spirit of this invention.

Claims

1. A method of manufacturing a semiconductor device, comprising a semiconducting substrate in the shape of a slice, said semiconducting substrate, the method comprising the steps of:

step 1) selectively applying a pattern of a solid-based dopant source to a first major surface of said semiconducting substrate;

step 2) diffusing the dopant atoms from said

solids-based dopant source into said substrate by a controlled heat treatment step in a gaseous environment surrounding said semiconducting substrate, the dopant from said solids-based dopant source diffusing directly into said substrate to form a first diffusion region in said substrate immediately beneath said pattern of said solids-based dopant source and, at the same time, diffusing said dopant from said solids-based dopant source indirectly via said gaseous environment into said substrate to form a second diffusion region in at least some areas of said substrate not covered by said pattern; and

step 3) forming a metal contact pattern substantially in alignment with said first diffusion region without having etched said second diffusion region substantially.

2. A method according to claim 1, wherein said substrate is of the first conductivity type and the dopant of said solids-based dopant source is of a second conductivity type.
3. A method according to claim 1 or 2, further comprising the step of applying a passivating layer after said diffusing step 2) and before said metal contact forming step 3).
4. A method according to claim 3, wherein said passivating layer is an oxide layer.
5. A method according any of claims 1 to 4, further comprising the step of texturising said semiconducting substrate before the selective dopant source application step 1).
6. A method according to any of the preceding claims wherein said solids-based dopant source is a first paste applied by screen printing.
7. A method according to any of the preceding claims, further comprising the step of applying an anti-reflection coating.
8. A method according to claims 3 or 4, or 7, wherein said step 3) of forming a metal contact pattern includes forming ohmic contacts between said metal contact pattern and said first diffusion regions by sintering through said passivating and/or said anti-reflection coating.
9. A method according any of the preceding claims, wherein said selective dopant source application step 1) includes applying one or more further solids-based materials to one or more major surfaces of said substrate, each of said further solids-based

materials being a further dopant source of the same conductivity type as the said solids-based dopant source but with a different concentration, or being a further dopant source of another conductivity type or being undoped.

10. A semiconductor device manufactured according to the method of any of the claims 1 to 9, comprising a semiconducting substrate in the shape of a slice, a first doped region in one major surface, and a second doped region in said one major surface and abutting said first doped region, the doping level of said first and second doped regions decreasing monotonically from said first doped region to said second doped region.
11. A semiconductor device according to claim 10, wherein the ratio of the doping levels in said first and second regions is at least 5, and preferably about 10 or more.
12. A method according to any of claims 1 to 9 or a semiconductor device according to claim 10 or 11, wherein said semiconductor device is a photovoltaic cell.

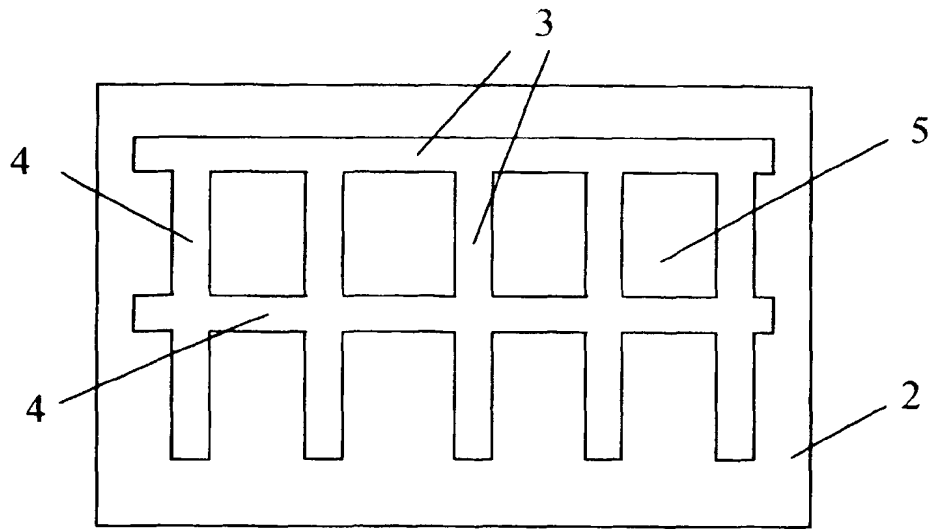


Fig. 1

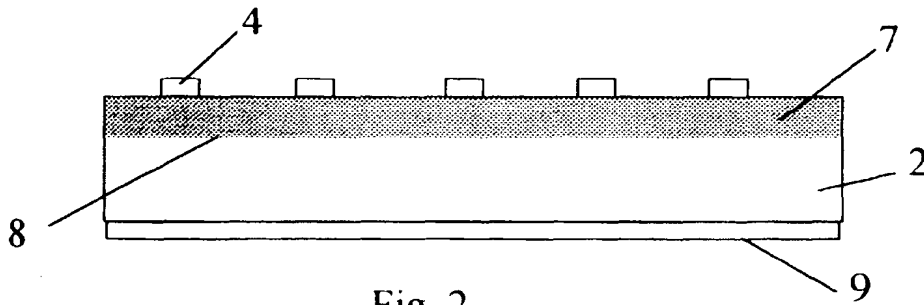


Fig. 2

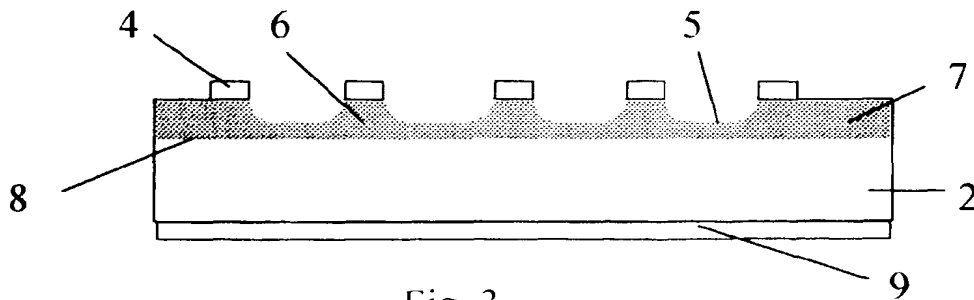


Fig. 3

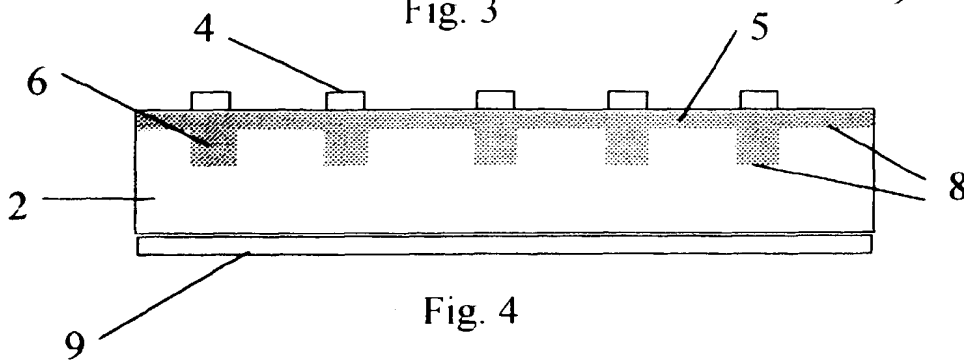


Fig. 4

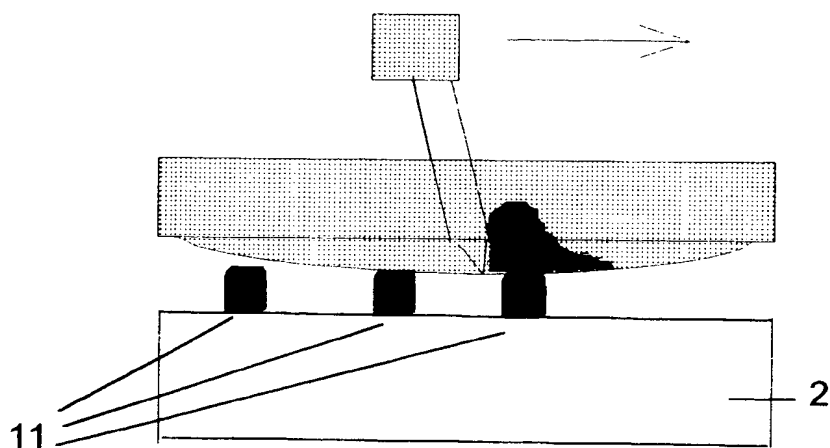


Fig. 5

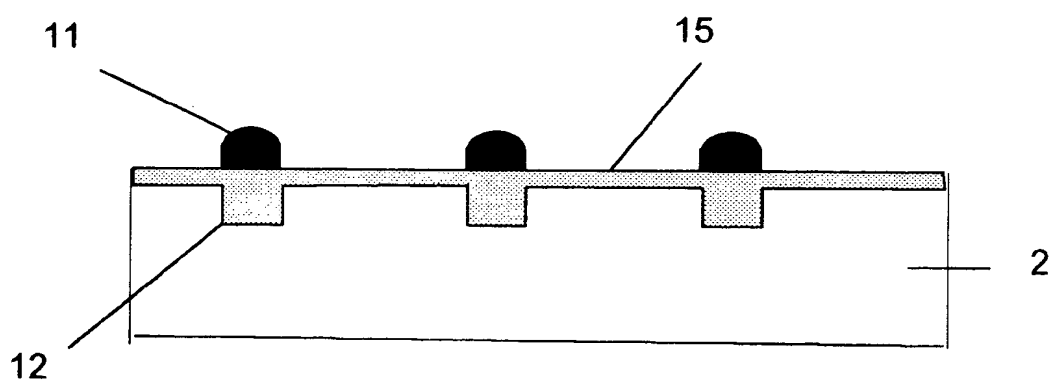


Fig. 6

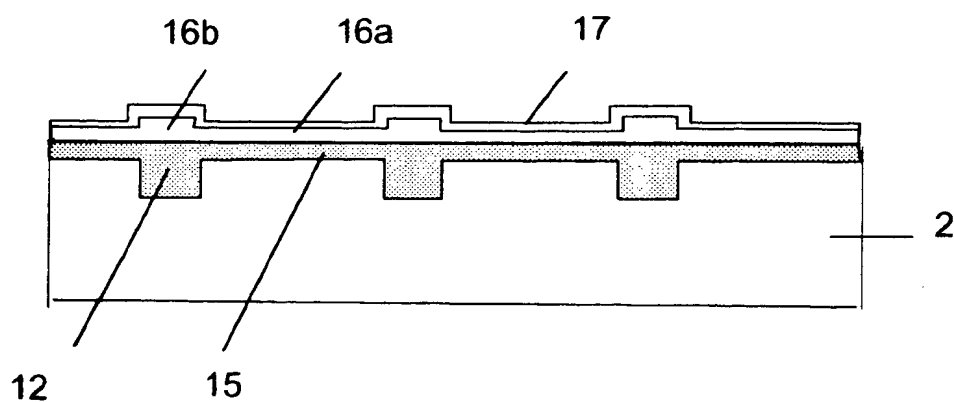


Fig. 7

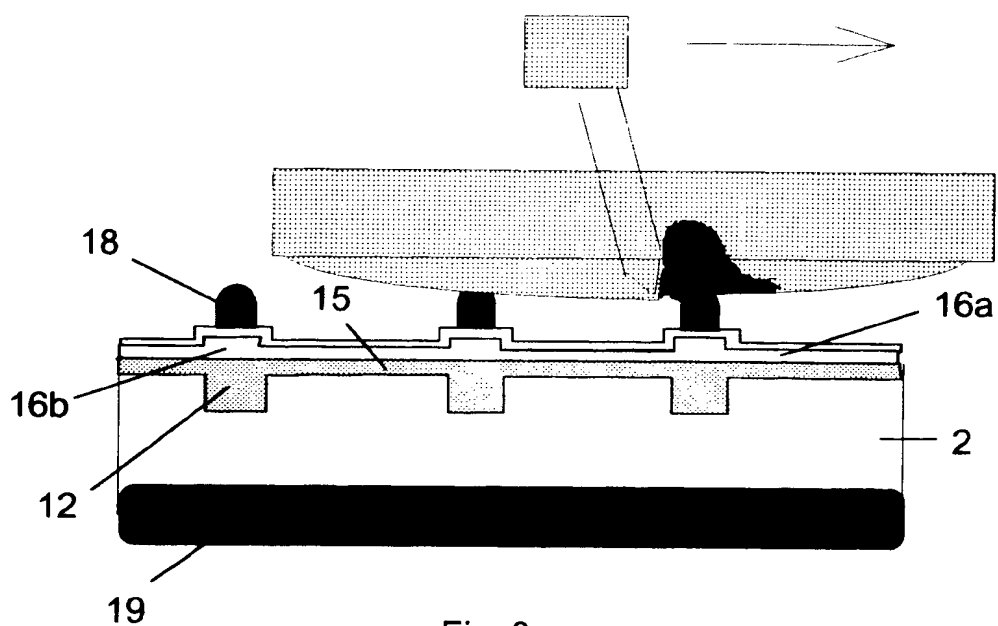


Fig. 8

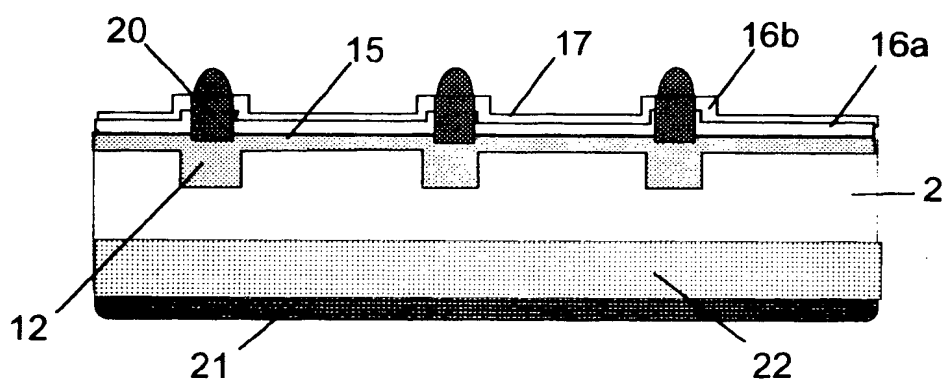


Fig. 9

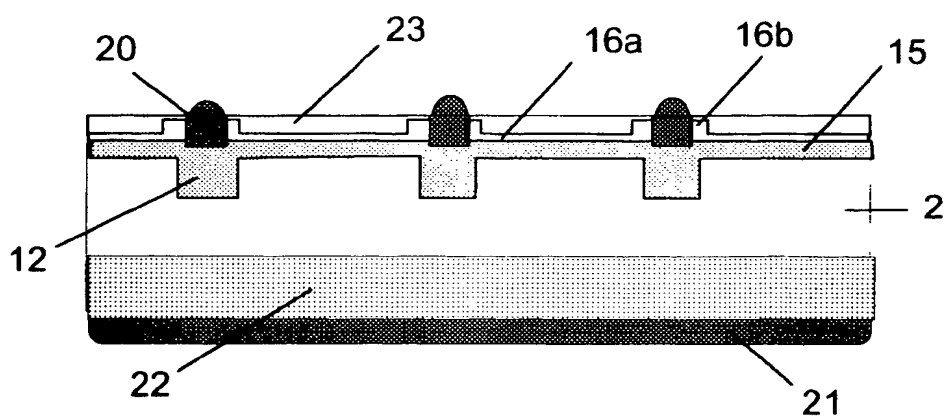


Fig. 10

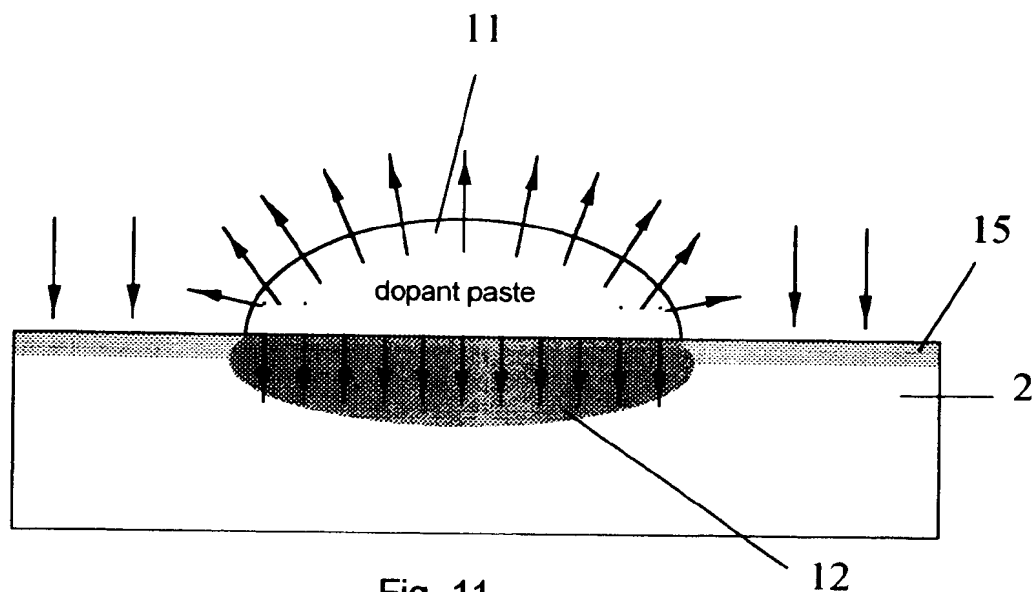


Fig. 11

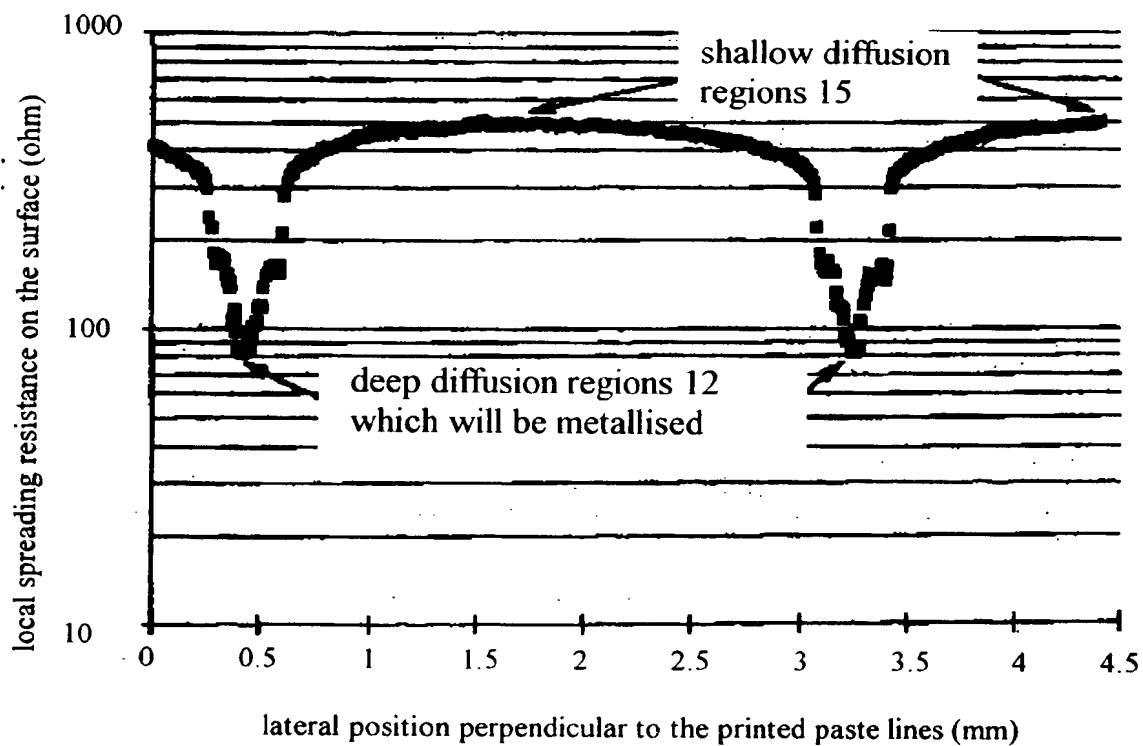


Fig. 12

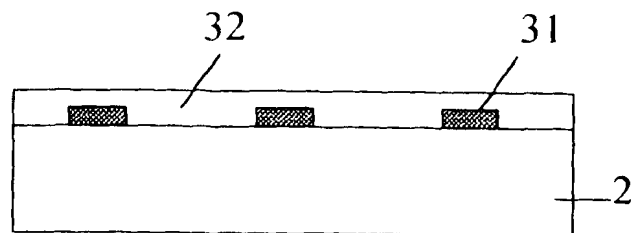


Fig. 13

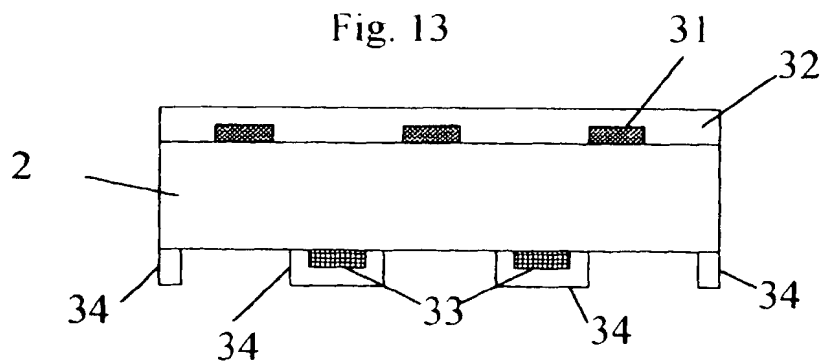


Fig. 14

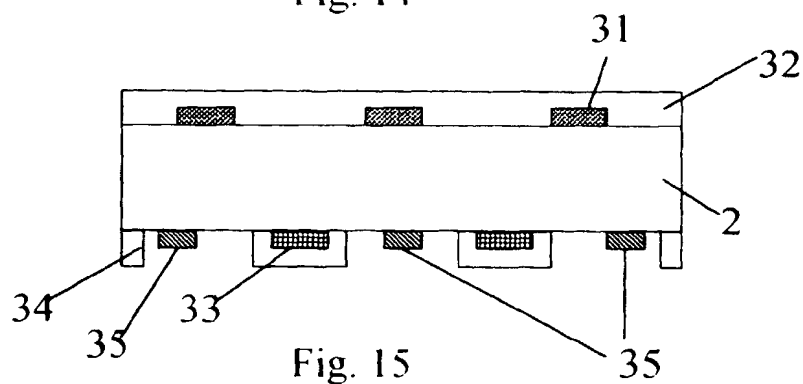


Fig. 15

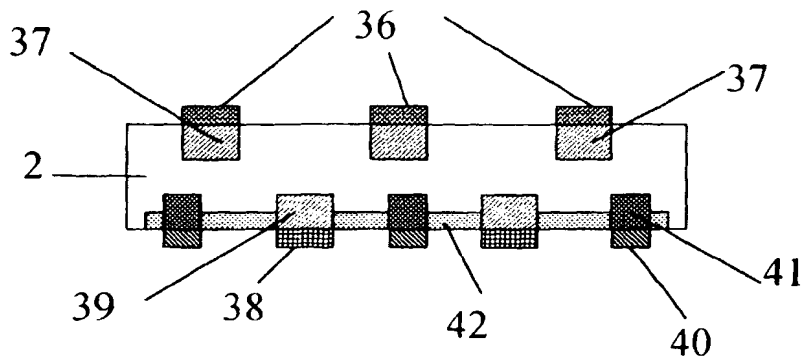


Fig. 16



European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 96 12 0865

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 4 152 824 A (GONSIORAWSKI RONALD) 8 May 1979 * abstract; figures 1-8 * * column 1, line 40 - line 60 * * column 2, line 39 - line 49 * * column 3, line 33 - line 43 * * column 5, line 38 - column 6, line 17 * * column 7, line 32 - line 41 * ---	1-4,7,9,12	H01L31/0224 H01L31/18
A	US 4 478 879 A (BARAONA COSMO R ET AL) 23 October 1984 * abstract; figures 1-4 * * column 2, line 43 - column 3, line 2 * ---	1,2,6	
A	IEEE ELECTRON DEVICE LETTERS, vol. 17, no. 8, 1 August 1996, pages 404-406, XP000597034 DOSHI P ET AL: "INTEGRATION OF SCREEN-PRINTING AND RAPID THERMAL PROCESSING TECHNOLOGIES FOR SILICON SOLAR CELL FABRICATION" * the whole document * ---	1,6,8	
A,D	DE 42 17 428 A (DEUTSCHE AEROSPACE) 17 June 1993 * column 1, line 15 - line 25 * * column 1, line 40 - line 61 * * column 2, line 49 - line 55 * * figures 1-3 * --- -/--	1-5,7,8,12	
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 21 May 1997	Examiner Visscher, E
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application I : document cited for other reasons & : member of the same patent family, corresponding document	
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			

EPO FORM 1503 03/92 (PWC01)



European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 96 12 0865

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A,D	APPLIED PHYSICS LETTERS, vol. 59, no. 13, 23 September 1991, pages 1583-1584, XP000235520 SZLUFCHIK J ET AL: "SIMPLE INTEGRAL SCREENPRINTING PROCESS FOR SELECTIVE EMITTER POLYCRYSTALLINE SILICON SOLAR CELLS" * page 1583, column 2, line 24 - column 3, line 12 * * figure 1 *	1,6,12	
A,D	DE 44 01 782 A (DAIMLER BENZ AEROSPACE AG) 1 27 July 1995 * abstract; figures 1-3 *	1	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 21 May 1997	Examiner Visscher, E
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document</p>			

EPO FORM 1503 03/82 (P4/C01)

10/1/02



A DOCPHOENIX

APPL PARTS

IMIS
Internal Misc. Paper
LET.
Misc. Incoming Letter

371P
PCT Papers in a 371 Application

A...
Amendment Including Elections

ABST
Abstract

ADS
Application Data Sheet

AF/D
Affidavit or Exhibit Received

APPENDIX
Appendix

ARTIFACT
Artifact

BIB
Bib Data Sheet

CLM
Claim

COMPUTER
Computer Program Listing

CRFL
All CRF Papers for Backfile

DIST
Terminal Disclaimer Filed

DRW
Drawings

FOR
Foreign Reference

FRPR
Foreign Priority Papers

IDS
IDS Including 1449

NPL
Non-Patent Literature

OATH
Oath or Declaration

PET.
Petition

RETMAIL
Mail Returned by USPS

SEQLIST
Sequence Listing

SPEC
Specification

SPEC NO
Specification Not in English

TRNA
Transmittal New Application

CTNF
Count Non-Final

CTRS
Count Restriction

EXIN
Examiner Interview

M903
DO/EO Acceptance

M905
DO/EO Missing Requirement

NFDR
Formal Drawing Required

NOA
Notice of Allowance

PETDEC
Petition Decision

OUTGOING

CTMS
Misc. Office Action

1449
Signed 1449

892
892

ABN
Abandonment

APDEC
Board of Appeals Decision

APEA
Examiner Answer

CTAV
Count Advisory Action

CTEQ
Count Ex parte Quayle

CTFR
Count Final Rejection

INCOMING

AP.B
Appeal Brief

C.AD
Change of Address

N/AP
Notice of Appeal

PA..
Change in Power of Attorney

REM
Applicant Remarks in Amendment

XT/
Extension of Time filed separate

BACKFILE DOCUMENT INDEX SHEET

Internal

SRNT
Examiner Search Notes

CLMPTO
PTO Prepared Complete Claim Set

ECBOX
Evidence Copy Box Identification

WCLM
Claim Worksheet

WFEE
Fee Worksheet

File Wrapper

FWCLM
File Wrapper Claim

IIFW
File Wrapper Issue Information

SRFW
File Wrapper Search Info

